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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/804,346 | 03/19/2004 | Philip Neaves | DB001095-000 | 7009 |

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| EXAMINER | |
|---|---|
| RILEY, SHAWN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2838 | |

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/804,346 | NEAVES, PHILIP | |
| | Examiner | Art Unit | |
| | Shawn Riley | 2838 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 March 2004 filing*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/04&06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This application is in condition for allowance except for the following formal matters:

### *Specification*

1. Applicant(s) is(are) reminded of the proper content of an abstract of the disclosure.

The abstract should not refer to purported merits (Hence, the chip area occupied by the resistors in the circuit is substantially reduced when compared with the area occupied by the resistors in the prior art BGR circuit. The circuit provides a steady reference voltage with sub-1V supply and very low power consumption)or speculative applications of the invention and should not compare the invention with the prior art (The overall resistance in the present circuit is substantially lower than the resistance in the prior art BGR circuit of comparable performance). Correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. E.g., Low Resistance Bandgap reference circuit with resistive T-network. Correction is required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

### Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed bandgap reference circuit including a T-network includes: a first resistor having a first terminal and a second terminal, wherein said first terminal is electrically connected to said first input, a second resistor having a third terminal and a fourth terminal, wherein said third terminal is electrically connected to said second terminal and said fourth terminal is electrically connected to said second input, and a third resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is electrically connected to at least one of said second and said third terminals and said sixth terminal is electrically connected to a reference potential; and a transistor network having a third input and a second output, wherein said first output of said operational amplifier is electrically connected to said third input to generate a bandgap reference voltage at said second output.

2. Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed bandgap reference circuit comprising: a third CMOS transistor having a gate connected to said output, a source connected to said supply voltage, and a drain connected to a second resistor, wherein a bandgap reference voltage is obtained at said drain of said third CMOS transistor; the improvement comprises: a T-network of passive resistors connected between said first and said second inputs, wherein said T-network includes: a third resistor having a first terminal and a second terminal, wherein said first terminal is electrically connected to said first input, a fourth resistor having a third terminal and a fourth terminal, wherein said-third terminal is electrically connected to said second terminal and said fourth terminal is electrically connected to said second input, and a fifth resistor having a fifth terminal and a sixth terminal, wherein said fifth

terminal is electrically connected to at least one of said second and said third terminals and said sixth terminal is electrically connected to a reference potential.

3. Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed bandgap reference method including: a first resistor having a first terminal and a second terminal, wherein said first terminal is connected to said first input, a second resistor having a third terminal and a fourth terminal, wherein said third terminal is connected to said second terminal and said fourth terminal is connected to said second input, and a third resistor having a fifth terminal and a sixth terminal, wherein said fifth terminal is connected to at least one of said second and said third terminals and said sixth terminal is connected to a reference potential; and further providing a transistor network having a third input and a second output, wherein said first output of said operational amplifier is connected to said third input

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Allowable Subject Matter***

1. Claims 1-14 are allowable over the prior art of record.

***Conclusion***

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

June 05

*Shawn Riley*
*Primary Examiner*